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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,298	04/23/2001	Michitaka Urushima	NEC01P030-HSc	3167

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EXAMINER
GEYER, SCOTT B

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 10/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,298	URUSHIMA, MICHITAKA	
	Examiner	Art Unit	
	Scott B. Geyer	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 25-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 25-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. The election without traverse of claims 1-9 and 25 without traverse and cancellation of claims 10-24 by the applicant is noted.

Drawings

2. The submission of formal drawings by the applicant and entered as paper no. 5 is noted.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "stud bump has a surface which is lower that a surface of said adhesive layer" of claim 27 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 30 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 30 recites "said adhesive layer comprises a

thermoplastic PI region having a thickness of 50 μm". The specification does not define the meaning for "PI". The specification is also silent as to the meaning of "region" and to whether it covers the entire thickness of the adhesive layer or only a portion of the adhesive layer.

6. Claim 30 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 30 recites "said adhesive layer comprises a thermoplastic PI region having a thickness of 50 μm". The specification does not define the meaning for "PI". The specification is also silent as to the meaning of "region" and to whether it covers the entire thickness of the adhesive layer or only a portion of the adhesive layer.

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7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 27 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 27 recites a "stud bump has a surface which is lower that a surface of said adhesive layer". It is unclear as to what the applicant intends by a surface lower than the surface of the adhesive layer. Further, the drawings do not detail such a feature as noted above in paragraph 3. The claim has not been treated further on its merits.

Claim Rejections - 35 USC § 102

9. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

10. Claims 1, 9, 29 and 31 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by the Urushima (JP 05-003183).

As to ***claim 1***, Urushima teach a chip substrate 4, stud bumps 10 on the chip substrate, a protective film 12 on the chip substrate (on the same surface as the stud bumps 10) and wherein the stud bumps 10 project from the surface of the adhesive layer (see figure 1). Further, Urushima teach the protective film layer to be a layer of cured epoxy resin, which is an adhesive layer.

As to ***claim 9***, Urushima teach the adhesive layer composed of a cured epoxy resin (see abstract).

As to ***claim 29***, Urushima teach the protective film to be an epoxy resin which is cured (see abstract).

As to ***claim 31***, Urushima teaches stud bums 10 attached to the electrodes 11. Further, as to claim 31 which recites that the stud bump is "connected to said electrode via an ultrasonic weld", this limitation has not been given patentable weight, as the method limitation does not give breadth or scope and fails to further limit the product claim.

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11. Claims 5 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by the applicant's admission of prior art.

As to ***claim 5***, applicant's prior art figure 3 teaches a semiconductor chip (70) with an adhesive layer (98) on the surface of a chip and allowing bumps (80) to be exposed and electrically attach to a wiring pattern on an interposer (72B). The wiring pattern adheres to the adhesive layer. The opposite surface of the interposer has an insulating and covering layer which has openings for external connections (96) such as solder balls.

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12. Claim 25 is rejected under 35 U.S.C. 102(e) as being anticipated by Jackson (6,285,081 B1).

Jackson teaches a semiconductor chip (figure 1B, numeral 115) with an adhesive layer (130) provided on the surface of the chip with solder bumps (125). The solder bumps are exposed through the adhesive layer. A tape substrate (135) is used to connect the die to an interposer whereby the interposer is a circuit board (110). The chip is attached to the "front" side of the tape and the interposer is attached to the "back" side of the tape, and electrical connection is provided between the chip, tape and interposer by solder bumps (125) and (145).

Claim Rejections - 35 USC § 103

13. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

14. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urushima (JP 05-003183) as applied to claim 1 above, and further in view of applicant's admitted prior art.

As to ***claim 2***, Urushima teach a chip, stud bumps and an adhesive layer wherein the stud bumps project from the surface of the adhesive layer. Urushima does not specifically teach an interposer attached to the device of claim 1. However, applicant's admitted prior art teach a similar device in figure 3 wherein the chip is attached to an interposer. Further, as to claim 2 which recites that the interposer is "bonded through thermocompression bonding", this limitation has not been given patentable weight, as the method limitation does not give breadth or scope and fails to further limit the product claim. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the device of Urushima with an interposer as is taught by applicant's prior art so as to provide a suitable platform for attachment of the chip to another substrate, i.e. mother board or circuit board.

As to ***claim 4***, applicant's prior art figure 3 teaches an interposer (72B) with a device hole (96).

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15. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Capote et al. (1998 International Symposium on Advanced Packaging Materials).

As to ***claim 3***, applicant's prior art figure 2 teaches a semiconductor chip (11), a stud bump (13) and an adhesive layer of protection film (18). The stud bumps (13) project from the surface as they are exposed (figure 2d) and applicant's prior art figure 3 teaches a chip (70) with bumps (80) to be attached to an interposer (72B). Applicant's admitted prior art does not specifically teach a cured flux. However, Capote et al. teach

the use of fluxes in flip chip bonding of chips to substrates. Capote et al. further teach that the flux will be cured after re-flow of the solder balls is completed (see pages 6 and 7). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the device of applicant's admitted prior art with a flux as taught by Capote et al. so as to assist in the re-flow of the solder balls for proper attachment of the chip to the substrate, i.e. interposer.

As to ***claim 6***, applicant's prior art figure 3 teaches a semiconductor chip (70) with an adhesive layer (98), which can be a resin layer (applicant's disclosure, page 4, lines 3-16) on the surface of a chip and allowing bumps (80) to be exposed and electrically attach to a wiring pattern on an interposer (72B). The wiring pattern adheres to the adhesive layer. The opposite surface of the interposer has an insulating and covering layer which has openings for external connections (96) such as solder balls. Applicant's admitted prior art does not specifically teach a cured flux. However, Capote et al. teach the use of fluxes in flip chip bonding of chips to substrates. Capote et al. further teach that the flux will be cured after re-flow of the solder balls is completed (see pages 6 and 7). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the device of applicant's admitted prior art with a flux as taught by Capote et al. so as to assist in the re-flow of the solder balls for proper attachment of the chip to the substrate, i.e. interposer.

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16. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roldan et al. (6,005,292) in view of applicant's admission of prior art.

Roldan et al. teach a stacked chip arrangement wherein two chips (figure 2C, numerals 30 and 36) are brought together to form a device where the two chips are electrically connected to each other (figure 2D). The electrical connection is made between solder bumps (figure 2C, numerals 34 and 44). Roldan et al. do not teach an adhesive layer covering a surface of each chip where the solder bumps are exposed through the adhesive layer. However, the applicant's prior art figure 2 teaches a semiconductor chip (11), a stud bump (13) and an adhesive layer of protection film (18). The stud bumps (13) project from the surface as they are exposed (figure 2d). Further, Urushima teach the protective film layer to be a layer of cured epoxy resin, which is an adhesive layer. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the device of Roldan et al. with an adhesive layer as taught by the applicant's admitted prior art. The adhesive layer, incorporated into the device of Roldan et al., would provide an extra means of attachment for the two devices in addition to the re-flowed solder bumps (figure 2D), ensuring a better bond between the two devices. Also, the adhesive layer would provide protection to the electrical connection from environmental factors such as moisture.

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17. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mostafazadeh et al. (5,783,870) in view of applicant's admission of prior art.

Mostafazadeh et al. teach a stacked chip arrangement wherein multiple chips are stacked on top of one another (figure 4A). The chips are bonded using bond pads on the top surfaces and bottom surfaces of the chips and using solder balls to make

electrical connections between each chip (see figures 4B and 4C). Mostafazadeh et al. do not teach an adhesive layer covering a surface of each chip where the solder bumps are exposed through the adhesive layer. However, the applicant's prior art figure 2 teaches a semiconductor chip (11), a stud bump (13) and an adhesive layer of protection film (18). The stud bumps (13) project from the surface as they are exposed (figure 2d). Further, Urushima teach the protective film layer to be a layer of cured epoxy resin, which is an adhesive layer. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the device of Mostafazadeh et al. with an adhesive layer as taught by the applicant's admitted prior art. The adhesive layer, incorporated into the device stack of Mostafazadeh et al., would provide an extra means of attachment for the devices in addition to the solder bumps, ensuring a better bond between the devices. Also, the adhesive layer would provide protection to the electrical connection from environmental factors such as moisture.

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18. Claims 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urushima (JP 05-003183) as applied to claim 1 above, and further in view of Chakravorty (6,181,569 B1).

As to ***claim 26***, Urushima teaches stud bumps which project through the adhesive layer as stated above in the rejection of claim 1. Urushima does not explicitly teach the stud bumps "protruding" from the adhesive layer. However, Chakravorty teaches stud bumps (metal bumps) 313 projecting through a polymer encapsulant layer 312 in figure 8c and also teaches stud bumps (metal bumps) 314 protruding from the

polymer encapsulant layer 312 in figure 8d. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the device of Urushima with stud bumps that protrude from a surface as taught by Chakravorty so as to provide external electrical connectivity to another substrate or surface.

As to ***claim 28***, Chakravorty teach gold used to make stud bumps (metal bumps) (see column 9, lines 17-18).

Response to Arguments

19. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

20. Applicant's arguments filed 8-9-02 for claim 25 have been fully considered but they are not persuasive. Applicant asserts that Jackson does not teach an adhesive layer or a tape substrate and points to column 5 ,line 54. However,. Jackson does teach an adhesive layer and a tape substrate in column 6, lines 43-54. A tape substrate, which is also inherently an adhesive layer, is clearly disclosed and the tape substrate can also serve as an interposer.

Conclusion

21. This action is **NON-FINAL**.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer whose telephone number is (703) 306-5866. The examiner can normally be reached on weekdays, between 10:00am - 6:30pm. The examiner may also be reached via e-mail: scott.geyer@uspto.gov

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

S.B.G.
October 29, 2002

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